4.5.2 – 200 PIN SDRAM DIMM FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS

DATA CONFIGURATIONS—Four DATA Word configurations are defined:

—64 BIT without PARITY
—72 BIT for PARITY CODES
—72 BIT & 80 BIT for ECC CODES

CONFIGURATION—21 Different Configurations are defined using various combinationa of X1, X4, X8, X9, X16 and X18 SDRAM memory devices.

LOGIC FEATURES—The modules contain parallel “PRESENCE DETECT” and ”IDENTITY” features that conist of output pins in the PDn and IDn fields which supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

By revision in Release 11, an optional Differential Clock was added plus the option of incorporating Serial Presence Detect instead of Parallel Presence Detect.

PACKAGE—200 PIN JEDEC DIMM MEMORY MODULE

PIN ASSIGNMENTS AND PD TABLES—Figs. 4.5.2–A, 4.5.2–B, & 4.5.2–C

MECHANICAL KEY DEFINITION—Fig. 4.5.2–D

PIN DEFINITIONS—Fig. 4.5.2–E

CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.2–F through 4.5.2–M

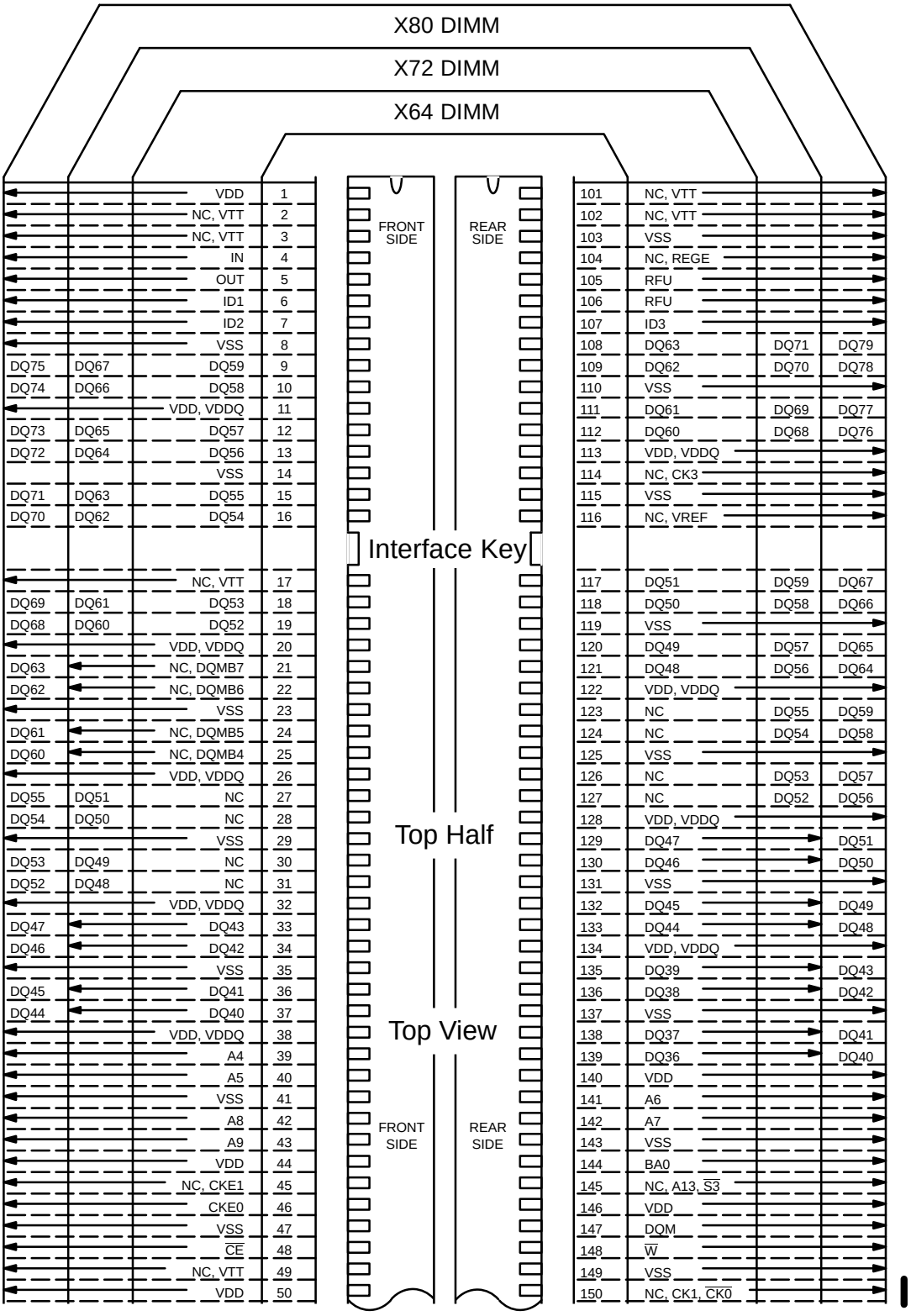


Figure 4.5.2–A
200 PIN, 64, 72, or 80 BIT SDRAM DIMM PINOUT, TOP HALF

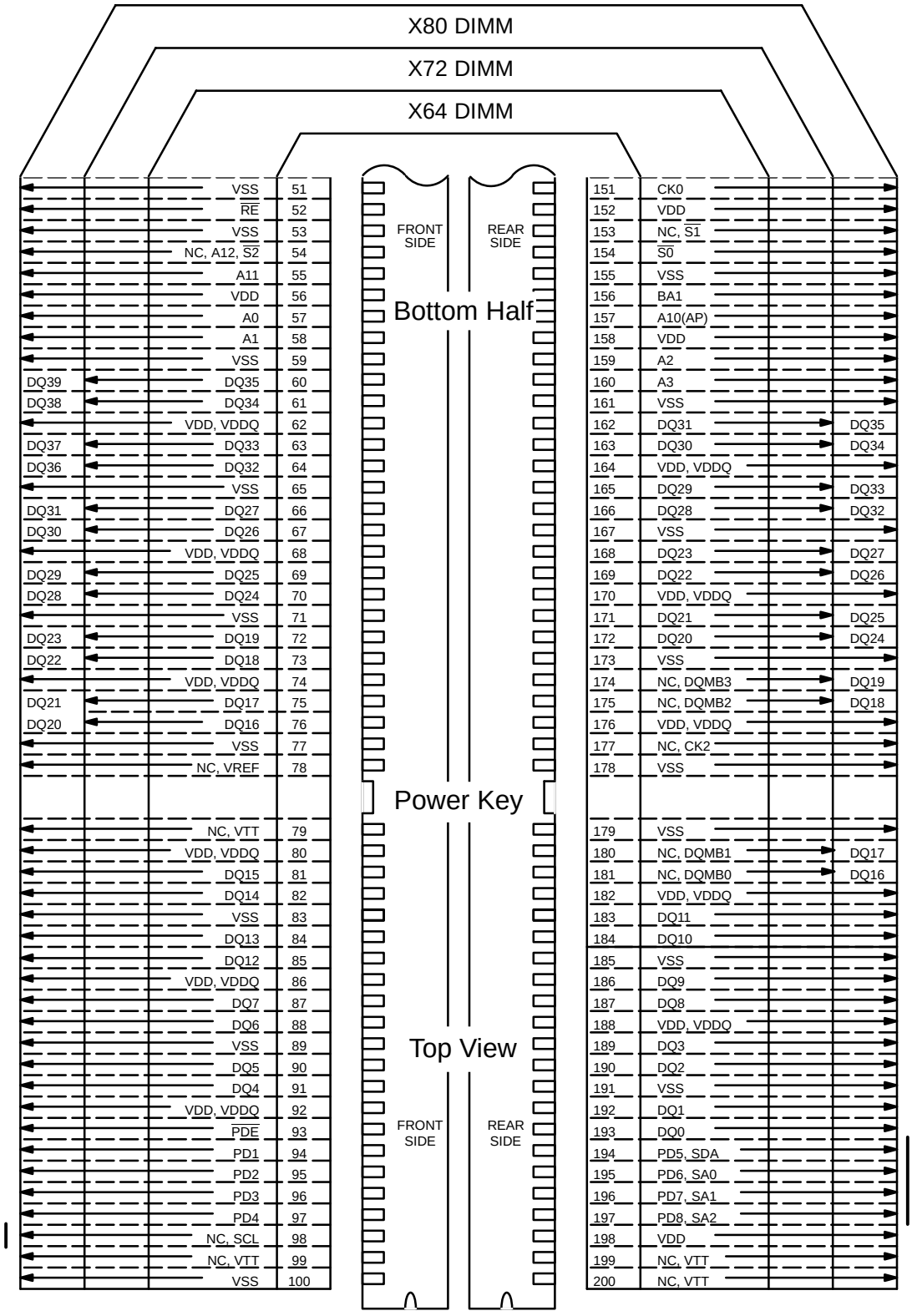


Figure 4.5.2–B
200 PIN, 64, 72, or 80 BIT SDRAM DIMM PINOUT, BOTTOM HALF

PD BITS 4 3 2 1	MODULE CONFIGURATION	SDRAM ORGANIZATION	RE ADDR.	CE ADDR
1 1 1 1	NO MODULE			
1 0 0 0 0 0 0 0	1M X 64/72/80 2M X 64/72/80	1M X 16 1M X 16	12 12	8 8
1 0 0 1 0 0 0 1	2M X 64/72/80 4M X 64/72/80	2M X 8 2M X 8	12 12	9 9
1 0 1 0 0 0 1 0	4M X 64/72/80 8M X 64/72/80	4M X 4/16 4M X 4/16	12 12	10 10
1 0 1 1 0 0 1 1	8M X 64/72/80 16M X 64/72/80	8M X 8 8M X 8	TBD TBD	TBD TBD
1 1 0 0 0 1 0 0	16M X 64/72/80 32M X 64/72/80	16M X 4 16M X 4	TBD TBD	TBD TBD
1 1 0 1 0 1 0 1	RFU RFU	TBD TBD	TBD TBD	TBD TBD
1 1 1 0 0 1 1 0	RFU RFU	TBD TBD	TBD TBD	TBD TBD
0 1 1 1	Expansion			.

Note 1 Presence Detect pins PD1—PD8 are buffered and enabled by $\overline{PDE}$. The ”1” outputs are NC and the ”0” outputs are driven low by on–module drivers when $\overline{PDE}$ is asserted active low.

Note 2 Buffered DIMMs (PD7=1) with PD8=0 (Byte–Write) shall be capable of both Word–Write and Byte–Write operations

	PD6	PD5
SPEED (tCYC)	195	194
15 ns	1	1
12 ns	1	0
10 ns	0	1
8 ns	0	0

PD SPEED TABLE

	PD7
INTERFACE	196
UNBUFFERED	0
BUFFERED	1

MODULE INTERFACE

	PD8
WRITE MODE	197
BYTE	0
WORD	1

WRITE MODE DETECT

	ID3
POWER	107
NORMAL	0
LOW–POWER	1

POWER LEVEL DETECT

	ID2
RAS TIMING	7
NO EARLY RAS	0
EARLY RAS	1

READ PRECHARGE TIMING

	ID1
INTERVAL	6
2 CLOCKS	0
1 CLOCK	1

COMMAND INTERVAL

Figure 4.5.2–C

200 PIN, 64, 72, or 80 BIT SIMM PRESENCE DETECT & CONFIGURATION TABLES

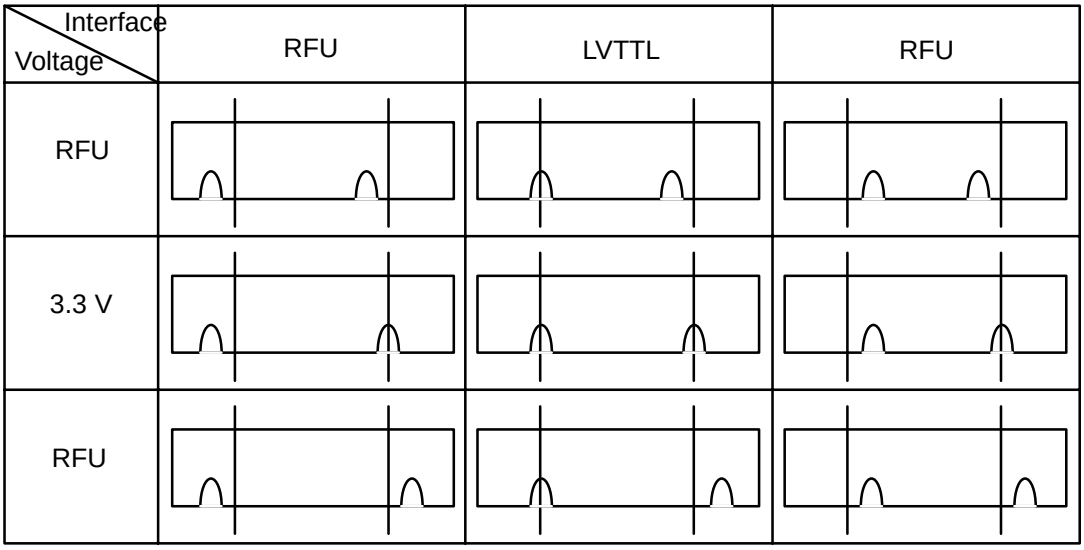


Figure 4.5.2–D

200 PIN, 8 BYTE SDRAM DIMM MECHANICAL KEY DEFINITION

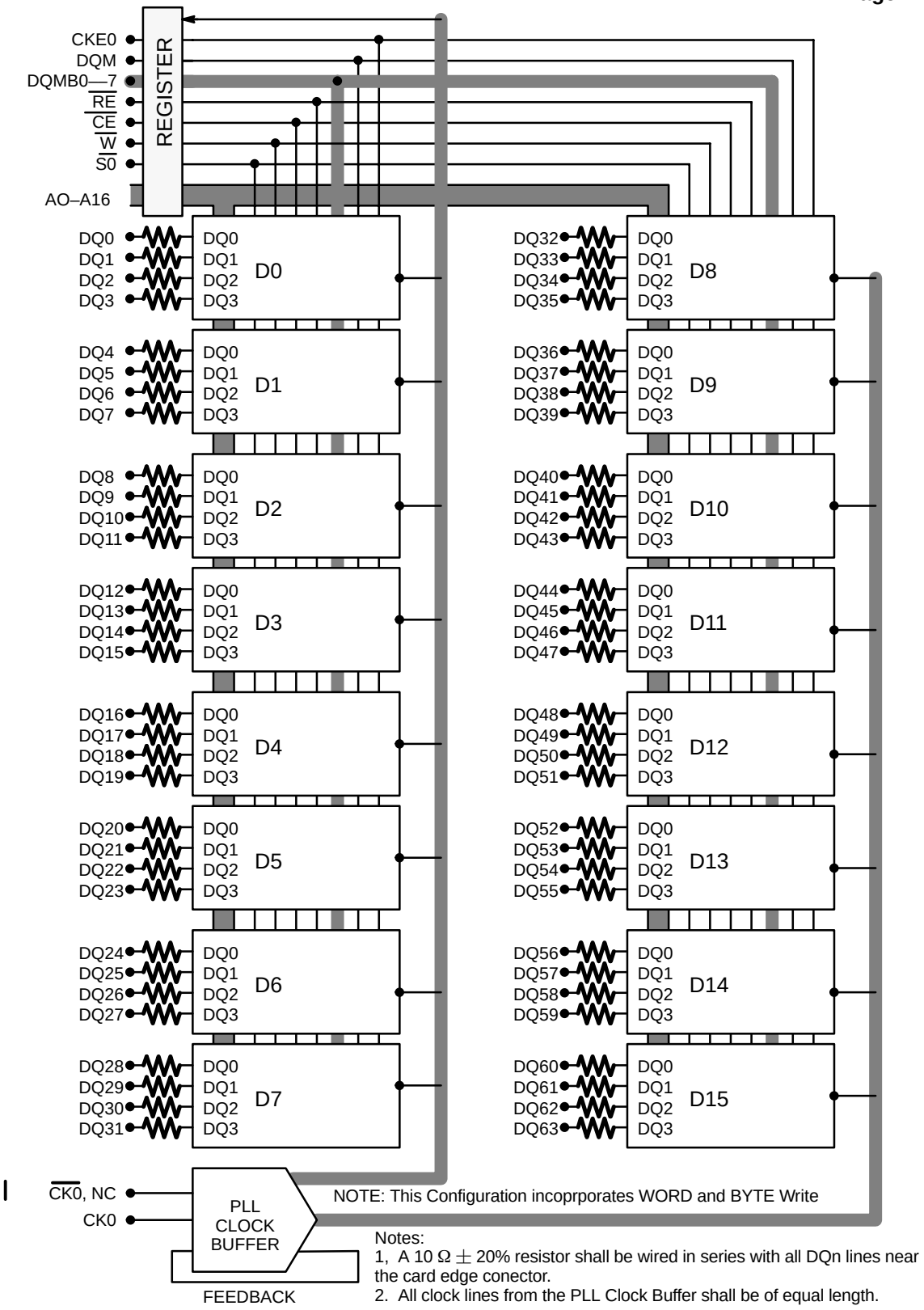
Pin Name	Number	Function
A0....A15	16	Address Input (multiplexed)
DQ0....DQ79	80	Data Input/Output (common)
CK0....CK3	4	Clock Input
CKE0....CKE1	2	Clock Enable Input
$\overline{S0}$....$\overline{S3}$	4	Chip Select Input
$\overline{RE}$	1	Row Enable (RAS) Input
$\overline{CE}$	1	Column Enable (CAS) Input
$\overline{W}$	1	Write Enable Input
DQM	1	Data Mask
DQMB0....DQMB7	8	Byte Data Mask
REGE	1	Buffer/Register Enable
$\overline{PDE}$	1	Presence Detect Enable
PD1....PD8	8	Buffered Logic Presence Detect Output
ID1....ID3	3	Identification Output
IN, OUT	2	Unbuffered Physical Detect Input/Output
VDD	9	Primary Positive Power Supply
VDDQ	20	Posivite Power for Input/Output
VREF	2	Reference Power Supply
VSS	33	Ground
VTT	11	Termination Power Supply
RFU	2	Reserved for Future Use

Notes:

1. Pin A14 is shared with S2, and pin A15 is shared with pin S3.
2 Pins DQMB0...DQMB7 are shared with pins defined as NC for X64 and X72 configurations.
3 REGE (Register Enable) operates similarly to the SAB pin on the 74AC11652 ”Octal Bus Transceiver and Register with 3–State Outputs”. When it is asserted, active high, the buffer–register operates in Register mode, as opposed to when it is de–asserted, inactive low, the buffer –register operates in ”real–time” buffer mode.
4. The unbuffered physical detect pins IN and OUT are shorted together on the DIMM.

Figure 4.5.2–E

8 BYTE SDRAM DIMM PIN DEFINITIONS



Notes:
1, A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.5.2–F

200 PIN, X64 BUFFERED SDRAM DIMM, 1 bank with X4 SDRAMs

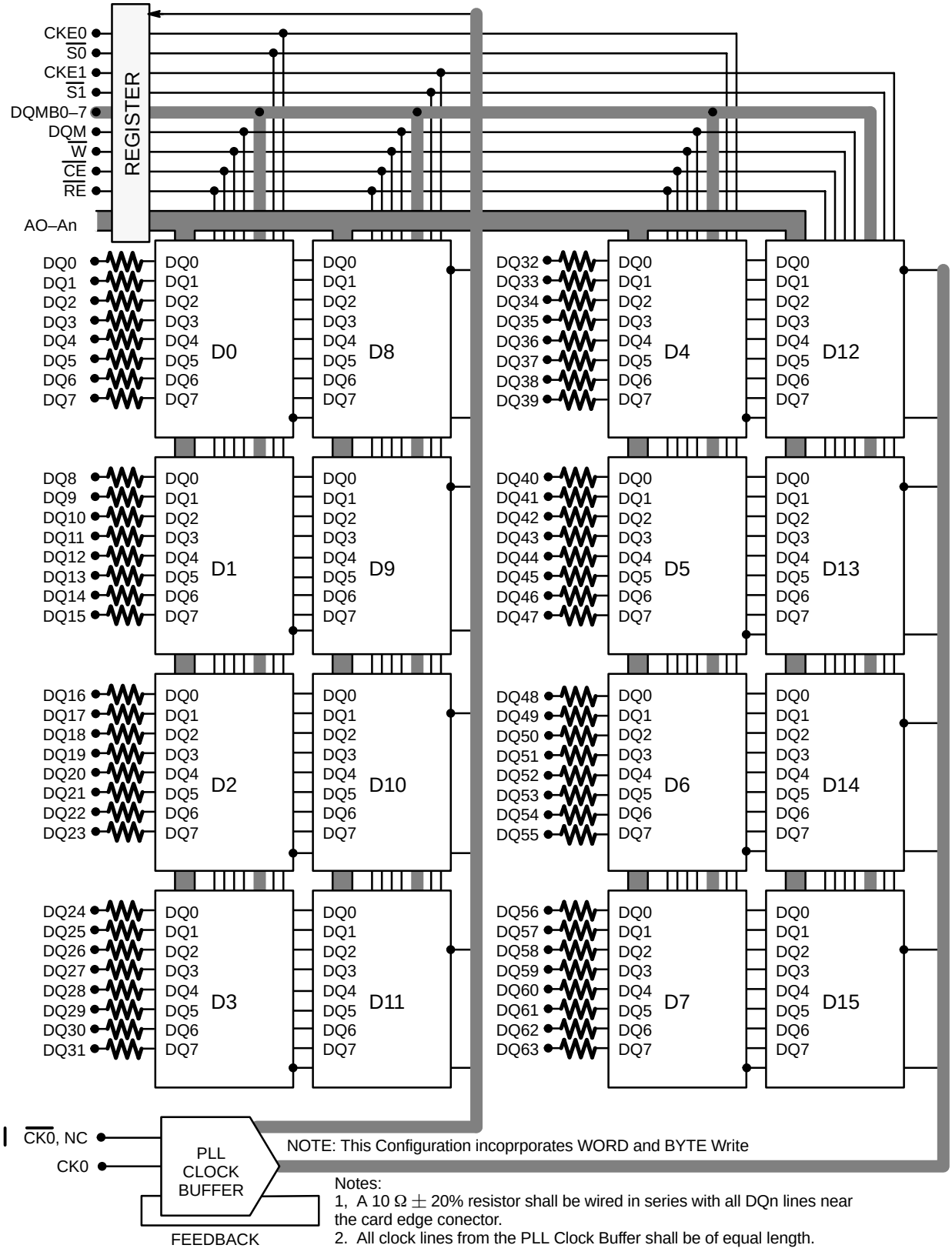


Figure 4.5.2–G

200 PIN, X64 BUFFERED SDRAM DIMM, 2 BANKS with X8 SDRAMs

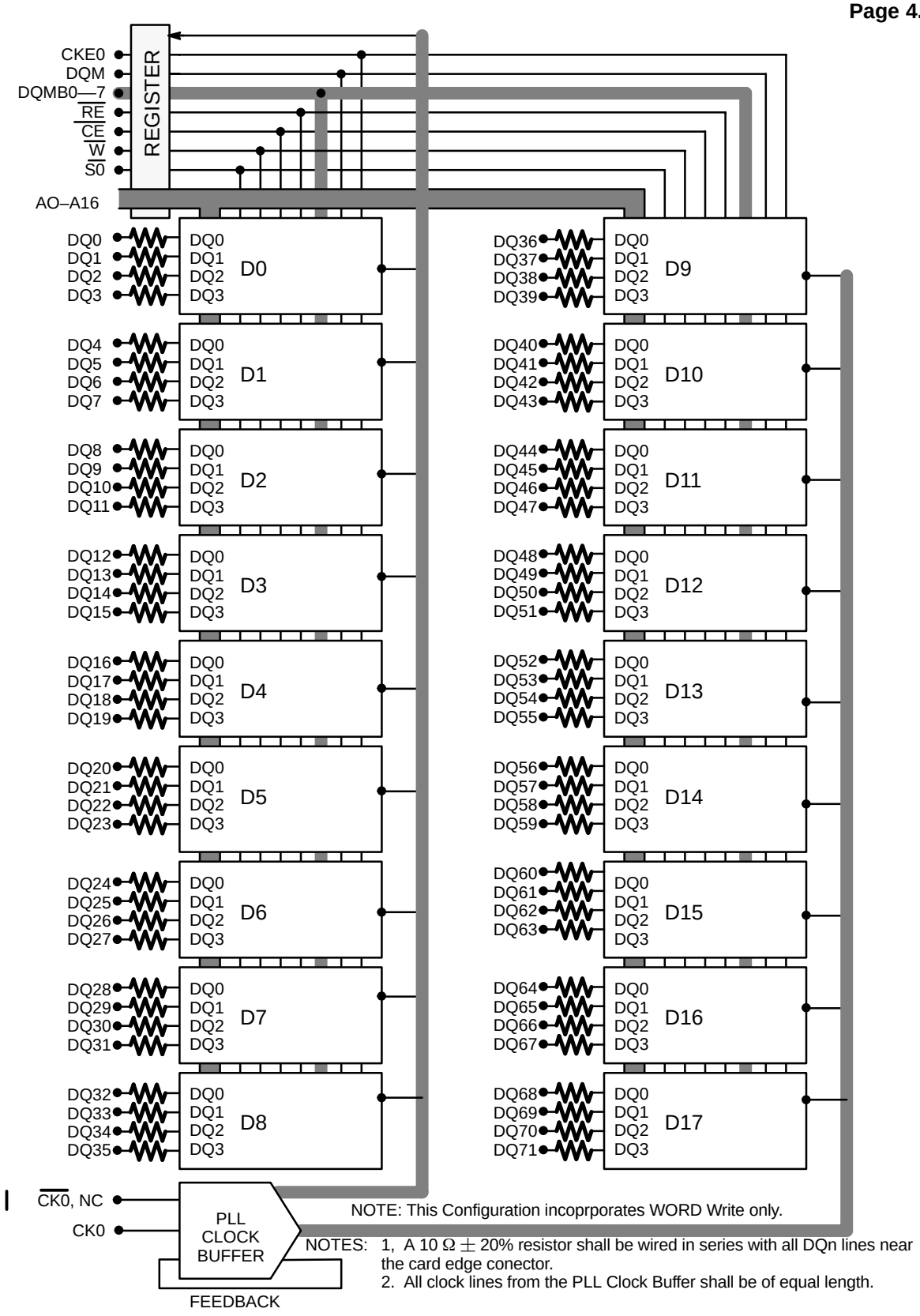
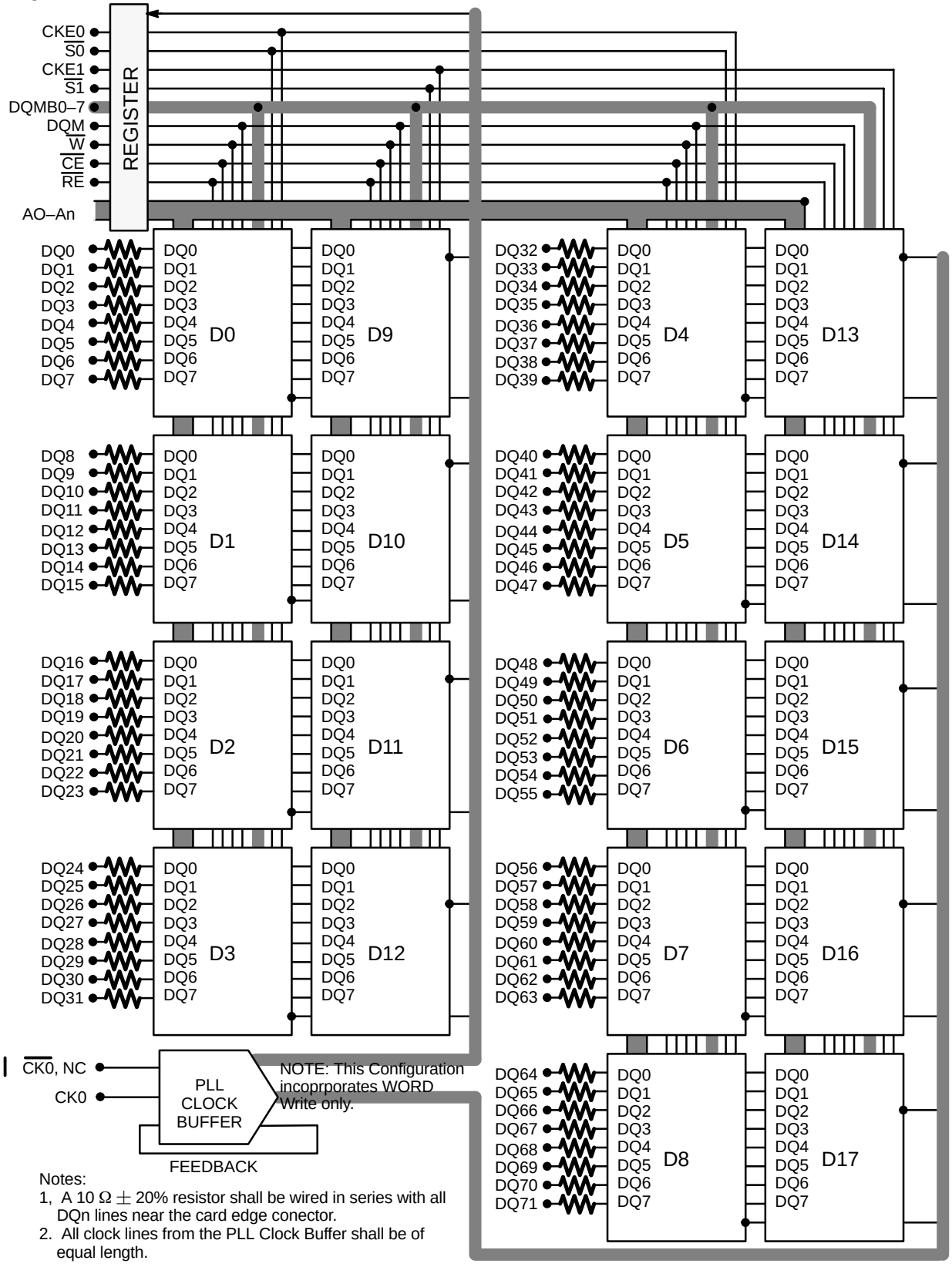


Figure 4.5.2–H

200 PIN, X72 BUFFERED SDRAM DIMM, 1 bank with X4 SDRAMs



Notes:
1, A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.5.2–I

200 PIN, X72 BUFFERED SDRAM DIMM, 2 BANKS with X8 SDRAMs

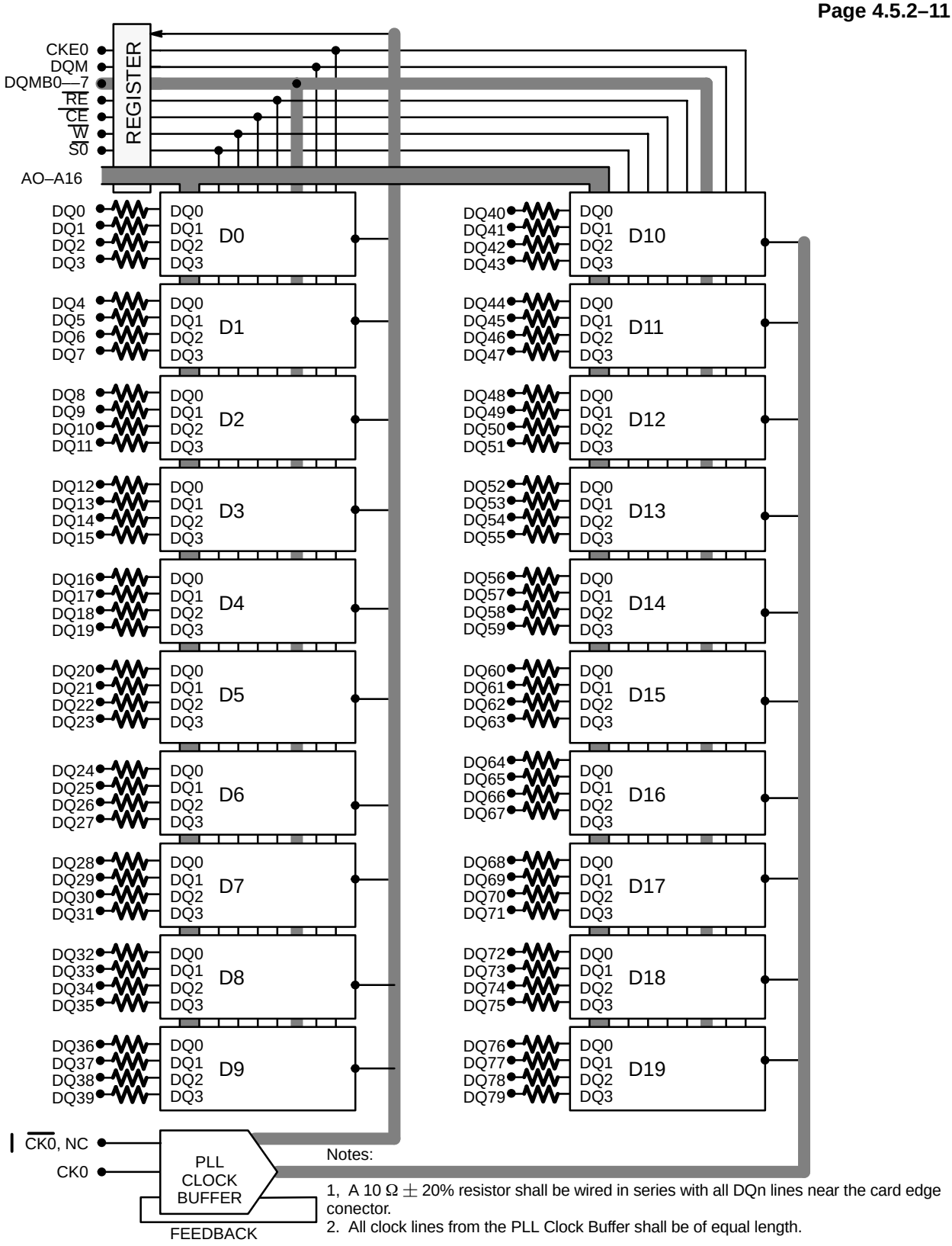
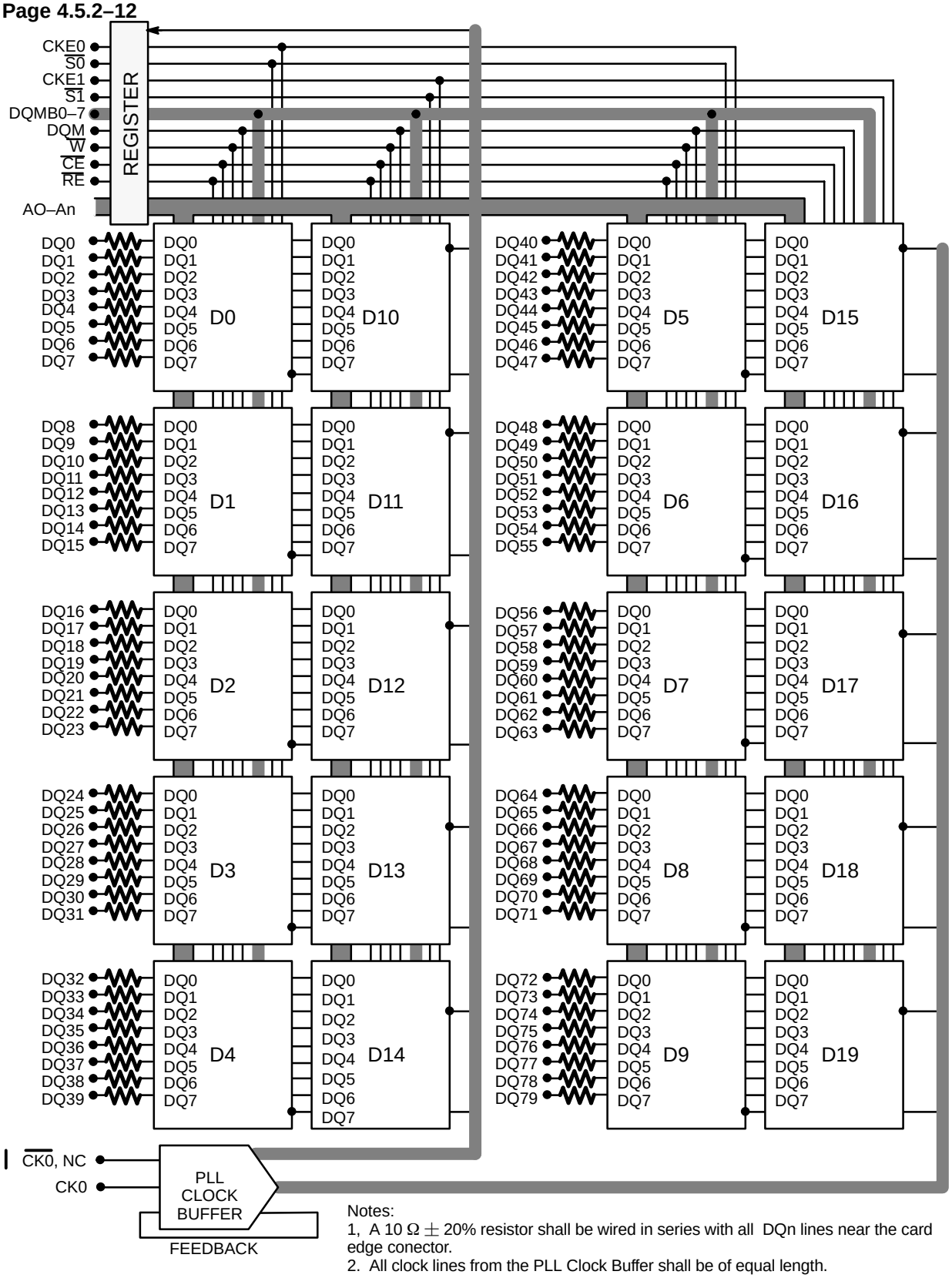


Figure 4.5.2–J

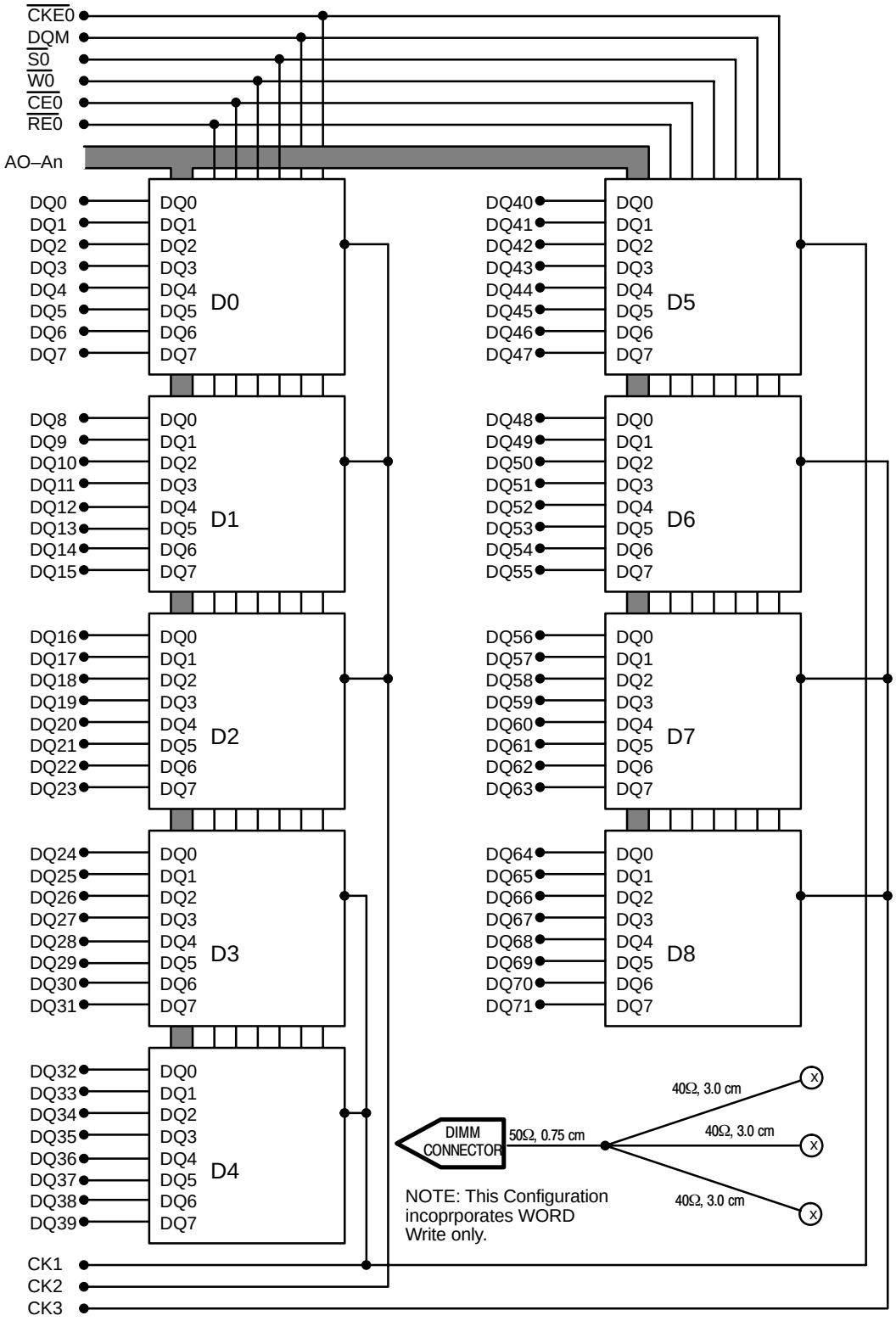
200 PIN, X80 BUFFERED SDRAM DIMM, 1 bank with X4 SDRAMs



Notes:
1, A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.5.2–K

200 PIN, X80 BUFFERED SDRAM DIMM, 2 BANKS with X8 SDRAMs



Note: All clock trees shall be routed as equal–length ”stars” from CK1, CK2, & CK3 inputs as shown in the diagram above.

Figure 4.5.2–L

200 PIN, X72 UNBUFFERED SDRAM DIMM, 1 bank with X8 DRAMs

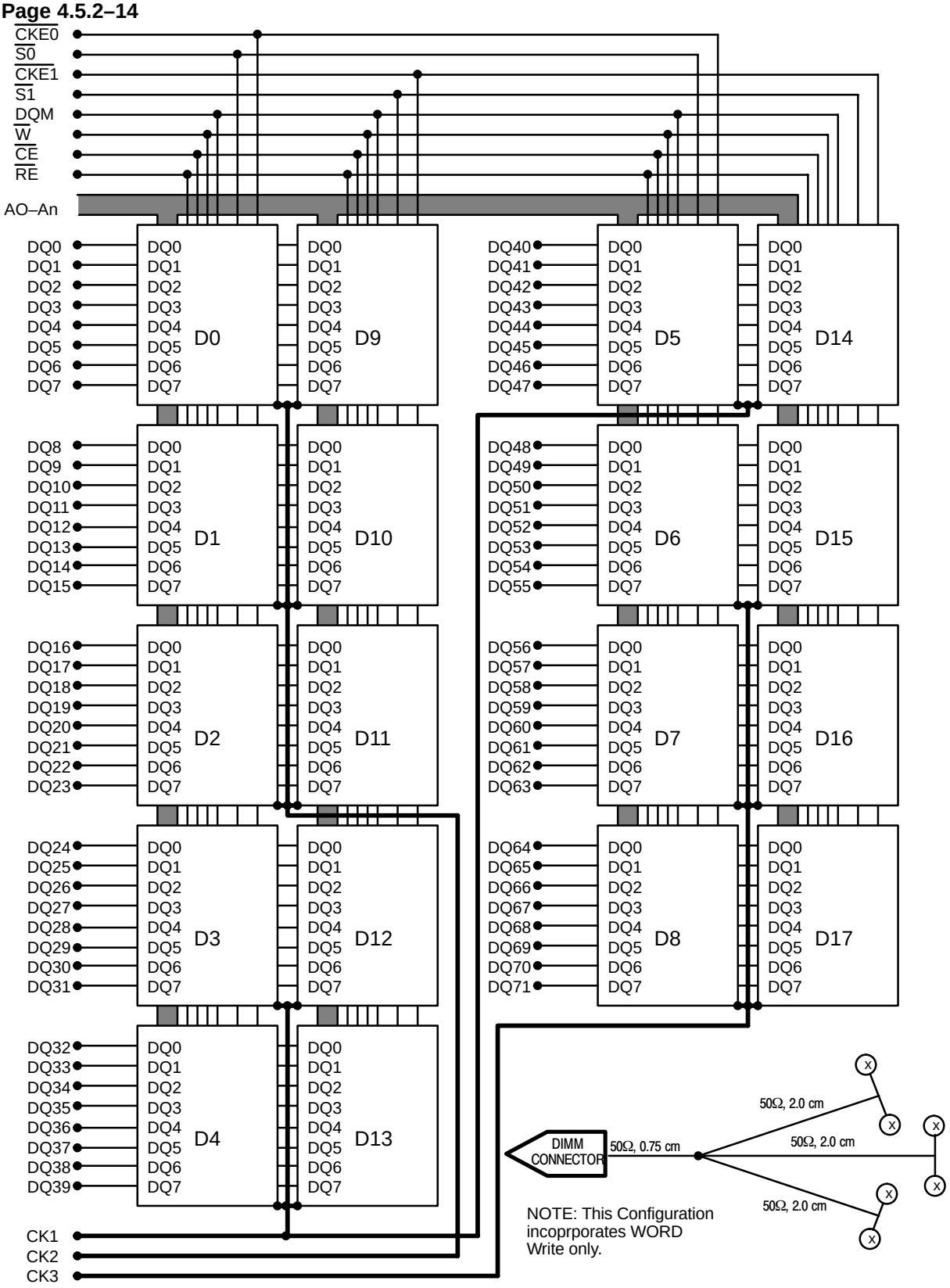


Figure 4.5.2–M

200 PIN, X72 UNBUFFERED SDRAM DIMM, 2 banks with X8 DRAMs